SPECIFICATION AMENDMENTS

Please amend the following paragraphs of the Specification as shown:

[0002] The present application is also related to U.S. Patent Application No. 10/613,825 ~~(Atty. Dkt. No. 029573-0301)~~ entitled VIRTUAL FINGER METHOD AND APPARATUS FOR PROCESSING DIGITAL COMMUNICATION SIGNALS, and U.S. Patent Application No. 10/613,477 ~~(Atty. Dkt. No. 029573-0501)~~ entitled SEARCHING METHOD AND APPARATUS FOR PROCESSING DIGITAL COMMUNICATION SIGNALS, both of which are assigned to the same assignee as the present application and are filed on an even date herewith.

[0010] Yet another drawback to the demodulator 10 is the design of static bit widths, which are set for worst-case operation. This design causes excessive power consumption when the full number of bits is not required for demodulation. Most of the time, ~~less~~ fewer bits are actually needed.

[0044] Another example of the dynamic processing ability of the processor 20 is the dynamic setting of bit-widths. Dynamically processing the bits is particularly beneficial ~~since less~~ because fewer bits are usually needed to produce a decodable output than the instantaneous worst case. By processing ~~less~~ fewer bits on average, less power is consumed.

[0055] Once all known multi-paths are estimated, channel estimates for a set of M relevant multi-paths are used in data de-spreading [[of]] in an operation 64. Notably, multi-paths can refer to communication signals from the one base station, other base stations, one antenna, or other antennas. In operation 64, data for path M is processed while multiplying by the channel estimate. Operation 64 continues until all relevant multi-paths for all channels are demodulated. In an operation 66, the processor sleeps until the next symbol group is available.

[0057] An address generator 52 decimates the samples to the correct rate and phase by initializing to the buffer address corresponding to the desired ~~sub-ship~~ sub-chip phase. To keep proper sub-chip phase alignment, the address generator 52 is advanced the number of sub-chips per access. A despreader 56 and a channel estimator 58 serially despread and accumulate the paths into a Symbol Buffer 54.

[0059] FIGURE 9 illustrates in more detail operations performed in the Accumulated Maximal Ratio Combining (A-MRC) procedure described with reference to FIGURE 6. In a state 62, [[an]] a multi-path counter, N, corresponding to which multi-path component is being processed, is set to zero. In a state 63, a pilot channel for path N is processed, yielding a channel estimate for path N. Pilot channel processing includes multiplying values from a sample buffer and a despread sequence generator. The samples from the pilot channel are accumulated and output to intermediate results buffers. As such, a channel ~~estimates~~ estimate is established for a path N. In a state 64, data for path N is despread and output to the intermediate results buffer.

[0060] In a state 65, the channel estimate for path N is multiplied by the despread data of path N, the accumulator is bypassed, and the output is sent to intermediate buffers. In a state 66, symbols from the path N are accumulated over multi-paths and base stations. The current MRC accumulation of the group of symbols (which are initialized to zero for processing of the first path) from the intermediate buffer are added to the despread and channel estimated symbols from the intermediate buffer, the accumulator is bypassed, and output is sent to intermediate buffers. States 63-66 are repeated until all N relevant multi-paths and base stations are processed at which point, the current MRC accumulation is the final accumulation and this value is output to the symbol processor. Advantageously, this process may be repeated in the case where a receiver is demodulating several channels. After that, in a state 67, the processor 20 sleeps until the next processing interval.

[0070] FIGURE 13 illustrates a receiver 75 supporting full-fledged MIMO. The receiver 75 treats paths emerging from different BS antennas as well as paths coming from different RX antennas almost the same as another multi-path. With respect to MI, the only addition to the receiver 75 compared to the processing system of FIGURE 7 is the necessity of a transformer 77 to handle such operations as STTD in WCDMA. Thus, the A-MRC algorithm can be almost exactly applied for MI with the difference that twice the number of paths could potentially be processed. With respect to MO, the only addition to the receiver 75 compared to theprocessing system of FIGURE 7 is that the sample ~~buffer~~ buffers 22 [[is]] are doubled to support data coming in from both RF chains. As a result, there is substantial cost savings. With respect to MI, there is no need of an additional multiplier. With respect to MO, additional fingers are not needed. There is also substantial power savings. The processor 20 is not forced to process all combinations of transmit/receive paths in the fingers. Only those antenna paths that are sufficiently strong need to be processed.